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(54) Phase change memory cell and manufacturing method thereof using minitrenches

(57) The phase change memory cell (5) is formed by a resistive element (22) and by a memory region (38) of a phase change material. The resistive element has a first thin portion having a first sublithographic dimension in a first direction (Y) ; and the memory region (38) has a second thin portion (38a) having a second sublithographic dimension in a second direction (X) transverse to the first dimension. The first thin portion (22) and the second thin portion (38a) are in direct electrical contact and define a contact area (58) of sublithographic extension. The second thin portion (38a) is delimited laterally by oxide spacer portions (55a) surrounded by a mold layer (49) which defines a lithographic opening (51). The spacer portions (55a) are formed after forming the lithographic opening, by a spacer formation technique.

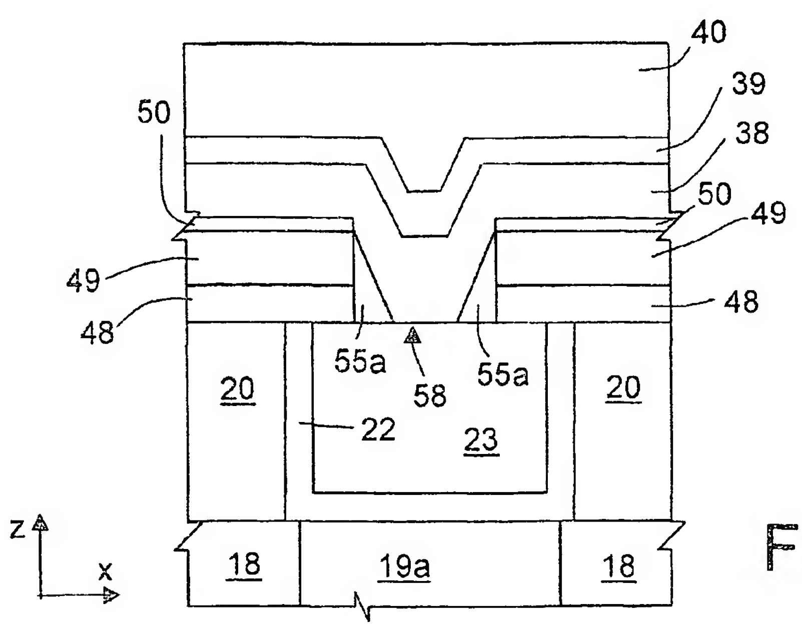


Fig.23

Description

[0001] The present invention relates to a phase change memory cell and to a manufacturing process thereof.

[0002] As is known, phase change memory (PCM) elements exploit the characteristics of materials which have the property of changing between two phases having distinct electrical characteristics. For example, these materials may change from an amorphous phase, which is disorderly, to a crystalline or polycrystalline phase, which is orderly, and the two phases are associated to considerably different resistivity.

[0003] At present, alloys of group VI of the periodic table, such as Te or Se, referred to as chalcogenides or chalcogenic materials, can advantageously be used in phase change cells. The chalcogenide that currently offers the most promise is formed by a Ge, Sb and Te alloy ($Ge_2Sb_2Te_5$), which is currently widely used for storing information in overwritable disks.

[0004] In chalcogenides, the resistivity varies by two or more magnitude orders when the material passes from the amorphous phase (more resistive) to the polycrystalline phase (more conductive) and vice versa. The characteristics of chalcogenides in the two phases are shown in Figure 1. As may be noted, at a given read voltage, here designated by Vr, there is a resistance variation of more than 10.

[0005] Phase change may be obtained by locally increasing the temperature, as shown in Figure 2. Below 150°C both phases are stable. Above 200°C (temperature of start of nucleation, designated by T_x), fast nucleation of the crystallites takes place, and, if the material is kept at the crystallization temperature for a sufficient length of time (time t_2), it changes its phase and becomes crystalline. To bring the chalcogenide back into the amorphous state, it is necessary to raise the temperature above the melting temperature T_m (approximately 600°C) and then to cool the chalcogenide off rapidly (time t_1).

[0006] From the electrical standpoint, it is possible to reach both critical temperatures, namely the crystallization temperature and the melting point, by causing a current to flow through a resistive element which heats the chalcogenic material by the Joule effect.

[0007] The basic structure of a PCM element 1 which operates according to the principles described above is shown in Figure 3 and comprises a resistive element 2 (heater) and a programmable element 3. The programmable element 3 is made of a chalcogenide and is normally in the polycrystalline state in order to enable a good flow of current. One part of the programmable element 3 is in direct contact with the resistive element 2 and forms the area affected by phase change, hereinafter referred to as the phase change portion 4.

[0008] If an electric current having an appropriate value is caused to pass through the resistive element 2, it is possible to heat the phase change portion 4 selectively up to the crystallization temperature or to the melting temperature and to cause phase change. In particular, if a current I flows through a resistive element 2 having resistance R, the heat generated is equal to I^2R.

[0009] The use of the PCM element of Figure 3 for forming memory cells has already been proposed. In order to prevent noise caused by adjacent memory cells, the PCM element is generally associated to a selection element, such a MOS transistor, a bipolar transistor, or a diode.

[0010] All the known approaches are, however, disadvantageous due to the difficulty in finding solutions that meet present requirements as regards capacity for withstanding the operating currents and voltages, as well as functionality and compatibility with present CMOS technologies.

[0011] In particular, considerations of a technological and electrical nature impose the creation of a contact area of small dimensions, preferably 20 nm x 20 nm, between the chalcogenic region and a resistive element. However, these dimensions are much smaller than those that can be obtained with current optical (UV) lithographic techniques, which scarcely reach 100 linear nm.

[0012] To solve the above problem, patent application 01128461.9, filed on 5.12.2001, and entitled "Small area contact region, high efficiency phase change memory cell, and manufacturing method thereof", teaches forming the contact area as an intersection of two thin portions extending transversely with respect to one another and each of a sublithographic size. In order to form the thin portions, deposition of layers is adopted instead of a lithographic process, given that deposition makes it possible to obtain very thin layers, i.e., having a thickness much smaller than the current minimum size that can be achieved using lithographic techniques.

[0013] For a better understanding of the problem of the present invention, the manufacturing process object of the above mentioned patent application No. 01128461.9 will now be described.

[0014] With reference to Figure 4, initially a wafer 10 comprising a P-type substrate 11 is subjected to standard front end steps. In particular, inside the substrate 11 insulation regions 12 are formed and delimit active areas 16; then, in succession, N-type base regions 13, N^+-type base contact regions 14, and P^+-type emitter regions 15 are implanted. The base regions 13, base contact regions 14, and emitter regions 15 form diodes that form selection elements for the memory cells.

[0015] Next, a first dielectric layer 18 is deposited and planarized; openings are formed in the first dielectric layer 18 above the base contact regions 13 and emitter regions 15, and the openings are filled with tungsten to form base contacts 19b and emitter contacts 19a. The base contacts 19b are thus in direct electrical contact with the base contact regions 13, and the emitter contacts 19a are in direct electrical contact with the emitter regions 15. Advantageously, the openings in the first di-

electric layer 18 can be covered by a barrier layer, for example a Ti/TiN layer, before being filled with tungsten. In this way, the structure of Figure 4 is obtained.

[0016] Figure 5 shows the layout of some masks used for forming the structure of Figure 4 regarding a pair of memory cells 5 that are adjacent in a perpendicular direction to the sectional plane of Figure 4 (Y direction). In particular, the figure shows a mask A used for defining the active areas 16, a mask B used for implanting the emitter regions 15, and a mask C for forming the openings where the base contacts 19b and the emitter contacts 19a are to be formed. Figure 4 is a cross-section taken along line IV-IV of Figure 5, while Figure 6 shows the same structure sectioned along the section line VI-VI of Figure 5.

[0017] Next (Figure 7), a second dielectric layer 20 -for example, an undoped silicon glass (USG) layer- is deposited, and openings 21 are formed in the second dielectric layer 20 above the emitter contact 19a. The openings 21 have dimensions dictated by the lithographic process and are, for example, circle-shaped. Next, a heating layer, for example of TiSiN, TiAlN or TiSiC, is deposited for a thickness of 10-50 nm, preferably 20 nm. The heating layer, designed to form the resistive element 2 of Figure 3, conformally coats the walls and bottom of the openings 21 and is subsequently removed outside the openings 21. The remaining portions of the heating layer thus form a cup-shaped region 22 and are then filled with dielectric material 23.

[0018] Next, as shown in the enlarged detail of Figure 8, a mold layer 27, for instance USG having a thickness of 20 nm, an adhesion layer 28, for instance Ti or Si with a thickness of 5 nm, and a first delimiting layer 29, for example nitride or another material that enables selective etching with respect to the adhesion layer 28, are deposited in sequence. The first delimiting layer 29 has a thickness of, for instance, 150 nm. Then, using a mask, one part of the first delimiting layer 29 is removed by dry etching to form a step which has a vertical side 30 that extends vertically on top of the dielectric material 23. The structure shown in Figure 8 is thus obtained.

[0019] Next (Figure 9), a sacrificial layer 31, for example TiN with a thickness of 30 nm, is deposited conformally. In particular, the sacrificial layer forms a vertical wall 31a that extends along the vertical side 30 of the first delimiting layer 29.

[0020] Next (Figure 10), the sacrificial layer 31 is undergoes an etch back that results in removal of the horizontal portions of the sacrificial layer 31 and of part of the vertical wall 31a. By appropriately choosing the thickness of the first delimiting layer 29 and the thickness of the sacrificial layer 31, as well as the time and type of etching, it is possible to obtain the desired sublithographic width W1 for the bottom part of the remaining vertical wall 31a.

[0021] As shown in Figure 11, a second delimiting layer 35, of the same material as the first delimiting layer 29, for example nitride, with a thickness of 300 nm, is deposited. Next, the delimiting layers 29, 35 and the vertical wall 31a are thinned by chemical mechanical polishing (CMP). At the end, the remaining portions of the delimiting layers 29, 35 form a hard mask, and the remaining portion of the vertical wall forms a sacrificial region 36.

[0022] Next (Figure 12), the sacrificial region 36 is removed. The adhesion layer 28 is isotropically etched, and the mold layer 27 is dry etched to form a slit 37 in the mold layer 27, the slit 37 having a width W1 equal to the width of the sacrificial region 36.

[0023] Next (Figure 13), the delimiting layers 29, 35 are removed, and a chalcogenic layer 38, for example of $Ge_2Sb_2Te_5$ with a thickness of 60 nm, is deposited conformally. The portion 38a of the chalcogenic layer 38 fills the slit 37 and forms, at the intersection with the cup-shaped region 22, a phase change region similar to the phase change portion 4 of Figure 3. Then, on top of the chalcogenic layer 38 a barrier layer 39, for example of Ti/TiN, and a metal layer 40, for example of AlCu, are deposited. The structure of Figure 13 is thus obtained.

[0024] Next (Figure 14), the stack formed by the metal layer 40, barrier layer 39, chalcogenic layer 38, and adhesion layer 28 is defined using a same mask to form a bit line 41. Finally, a third dielectric layer 42 is deposited, which is opened above the base contacts 19b. The openings thus formed are filled with tungsten to form top contacts 43 in order to prolong upwards the base contacts 19b. Then standard steps are performed for forming the connection lines for connection to the base contacts 19b and to the bits lines 41, and the final structure of Figure 14 is thus obtained.

[0025] In practice, as shown in Figure 15, the intersection between the cup-shaped region 22 and the thin portion 38a of the chalcogenic layer 38 forms a contact area 45 which is approximately square and has sublithographic dimensions. This is due to the fact that both the cup-shaped region 22 and the thin portion 38a have a width equal to the thickness of a deposited layer. In fact, the width of the cup-shaped region 22 is given by the thickness of the heating layer, and the width of the thin portions 38a is determined by the thickness of the sacrificial layer 31 along the vertical side 30. In greater detail, in the proximity of the contact area 45, the cup-shaped region 22 has a sublithographic dimension in a first direction (Y direction), and the thin portion 38a has a sublithographic dimension (width W1 of Figure 10) in a second direction (X direction) which is transverse to the first direction. Hereinafter, the term "sublithographic dimension" means a linear dimension smaller than the limit dimension achievable with current optical (UV) lithographic techniques, and hence smaller than 100 nm, preferably 50-60 nm, down to approximately 20 nm.

[0026] In the process described above, forming the thin portion 38a of the chalcogenic layer 38 entails numerous steps and is somewhat complex. Consequently, it is desirable to avail a simpler alternative process.

[0027] In addition, the dimensions of the contact area

45 depend upon the alignment tolerances between the mask used for forming the openings 21 and the mask used for removing part of the first delimiting layer 29 and for forming the vertical side 30 (Figure 8). In fact, as emerges clearly from a comparison between Figures 16a and 16b which are top plan views of the contact area 45, in the case of a cup-like region 22 having a circular shape and a diameter of approximately 0.2 μm, an alignment error of even only 0.05 μm between the two masks results in the thin portions 38a no longer crossing the cup-shaped regions 22 perpendicularly, with a consequent considerable increase in the dimensions of the contact area 45 (see Figure 16b) and hence a considerable increase in the flowing current, the value whereof would be uncontrollable.

[0028] Furthermore, the thin portion 38a crosses each cup-shaped region 22 in two points, thus doubling the total contact area between the thin portions 38a and the cup-shaped regions 22, and consequently also increasing the programming current. In the case of a marked misalignment between the two above masks, just one contact area is even obtained which has dimensions far greater than the requirements. The presence of a double contact gives rise to functional problems, given that in this situation it would be impossible to know which of the two contact areas 45 first causes switching of the overlying thin portion 38a (i.e., the phase change portion), nor would it be possible to be certain that both of the thin portions 38a overlying the two contact areas will switch.

[0029] The aim of the present invention is to simplify and improve the process described in patent application 01128461.9, with particular regard to forming the thin portion 38a.

[0030] According to the present invention there are provided a phase change memory element and a manufacturing process thereof, as defined in claims 1 and 9, respectively.

[0031] For a better understanding of the present invention, a preferred embodiment thereof is now described, purely by way of non-limiting example, with reference to the attached drawings, in which:

- Figure 1 shows the current versus voltage characteristic of a phase change material;
- Figure 2 shows the temperature versus current plot of a phase change material;
- Figure 3 shows the basic structure of a PCM memory element;
- Figure 4 shows a cross section of a wafer of semiconductor material in a manufacturing step of the cell of Figure 3, according to the aforementioned patent application;
- Figure 5 shows the layout of some masks used for forming the structure of Figure 4;
- Figure 6 is a cross-section taken along line VI-VI of Figure 5;
- Figures 7-14 are cross-section of the structure of the above mentioned patent application, in successive manufacture steps;
- Figure 15 is a top plan view, with parts removed and at an enlarged scale, of a detail of Figure 4;
- Figures 16a and 16b are top plan views, with parts removed, of a detail of Figure 14, in two different manufacture conditions;
- Figure 17 shows the layout of some masks used for forming the structure of Figure 7, according to the invention;
- Figure 18 is a cross-section similar to Figure 8, in a manufacture step according to the invention;
- Figure 19 shows the layout of some masks used for forming the structure of Figure 18;
- Figures 20 and 21 are cross-sections, similar to Figure 18, in successive manufacture steps according to the invention;
- Figure 22 is a top plan view of the structure of Figure 21;
- Figure 23 is a cross-section, similar to Figure 21, in a subsequent manufacture step;
- Figure 24 shows the layout of same masks used for forming the structure of Figure 23;
- Figure 25 is a cross-section, similar to Figure 14, in a final manufacture step according to the invention;
- Figures 26a and 26b are top plan views of the contact area, in two different manufacture conditions; and
- Figures 27 and 28 show two steps regarding a different embodiment.

[0032] In the following description, parts that are the same as those previously described with reference to Figures 4-14 are designated by the same reference numbers.

[0033] The process according to the present invention comprises initial steps equal to those described in patent application 01128461.9 illustrated above, up to deposition of the second dielectric layer 20 (Figure 7). Next, also here the openings 21 and the cup-shaped regions 22 are formed. However, as shown in Figure 17, for the definition of the openings 21, a heater mask D is used which has rectangular windows (the term "rectangular" also comprising the particular case of a square shape). Consequently, the openings 21 have a substantially rectangular shape. Then the heating layer, for example of TiSiN, TiAlN or TiSiC, with a thickness of 10-50 nm, preferably 20 nm, is deposited. The heating layer coats the walls and bottom of the openings 21 conformally. Consequently, in top plan view, the cup-like regions 22 here define an ideally rectangular shape, possibly with rounded edges (on account of the lithographic limits), or at the most an ovalized shape, with the longer side, or main direction, parallel to the X direction (Figure 22). Next, the heating layer is removed outside the openings 21 to form the cup-shaped regions 22, which are then filled with the dielectric material 23.

[0034] Then (Figure 18), a stop layer 48, for example

of nitride deposited by PECVD (Plasma Enhanced Chemical Vapor Deposition) with a thickness of 40 nm, a mold layer 49, for example of USG deposited by PECVD or SACVD (Sub-Atmospheric Chemical Vapor Deposition) with a thickness of 50-70 nm, and an adhesion layer 50, for example of Ti or Si with a thickness of 20-40 nm, are deposited in sequence.

[0035] Next, using a minitrench mask, designated by E in Figure 19, the adhesion layer 50, the mold layer 49 and the stop layer 48 are etched. As shown in Figure 19, the minitrench mask E has a rectangular window that extends between two adjacent cells 5 in the Y direction (perpendicular to the alignment direction of the base and emitter regions 14, 15 of each memory cell 5, Figure 7).

[0036] Following upon etching, part of the layers 48, 49 and 50 is removed, so as to form an opening 51 having a rectangular shape, corresponding to that of the minitrench mask E. The width of the opening 51 in the X direction is, for example, 160 nm. The opening 51 uncovers part of the dielectric material 23 of the two adjacent cells 5 and crosses each cup-shaped region 22 only once, as can be clearly seen from the superposition of the heater mask D and minitrench mask E in Figure 19.

[0037] Next, Figure 20, a spacer layer 55, for example an oxide layer, is deposited (in particular, TEOS with a thickness of 50 nm). The spacer layer 55 covers the adhesion layer 50, as well as the walls and bottom of the opening 51.

[0038] Then, Figure 21, the spacer layer 55 is anisotropically etched by etching back until the horizontal portions thereof are removed, according to the well known spacer formation technique. The spacer layer 55 is then completely removed above the adhesion layer 50 and is partially removed from the bottom of the opening 51 to form a spacer region 55a which extends along the vertical sides of the opening 51 (along the perimeter of a rectangle or of an oval) and delimits a slit 56, the base whereof forms a rectangular strip 57 having a sublithographic width W2 (in the X direction) of approximately 60 nm. Figure 22 is a top plan view of the structure thus obtained, and highlights how the strip 57 uncovers only one portion of the cup-shaped region 22 of each cell 5, shown with dashed line in the figure. The uncovered portion of each cup-shaped region 22 forms a contact area 58, as will be explained hereinafter.

[0039] Next, Figure 23, the chalcogenic layer 38 (also in the present case, for instance, of $Ge_2Sb_2Te_5$ with a thickness of 60 nm), the barrier layer 39, and the metal layer 40 are deposited in succession, to form a stack of layers 41. The chalcogenic layer 38 is in direct contact with the adhesion layer 50, to which it adheres properly, and fills the slit 56 with a thin portion 38a. In particular, the thin portion 38a of the chalcogenic layer 38 deposits on the strip 57, contacting the cup-shaped regions 22 at the contact areas 58. The inclined wall formed by the spacer region 55a favors filling of the slit 56, so preventing problems linked to a poor aspect ratio of the opening 51.

[0040] Next, the stack of layers 41 is defined using a stack mask F (Figure 24).

[0041] The process continues with the steps described previously, which comprise deposition of the third dielectric layer 42, opening of the third dielectric layer 42 above the base contacts 19b, formation of the top contacts 43, and formation of connection lines for connection to the base contacts 19b and to the bit lines 41, so as to obtain the final structure shown in Figure 25.

[0042] The advantages of the process and structure described herein are illustrated hereinafter. First, the sequence of steps required for forming the thin portion 38a is simplified, and the chalcogenic layer 38 adheres perfectly to the underlying layers and fills the opening 51 correctly, thanks to the inclination of the spacer region 55a, as already mentioned previously.

[0043] Furthermore, the shape of the minitrench mask E makes it possible to obtain a single contact area 58 for each cup-shaped region 22, and hence for each cell 5, without requiring any additional masking steps.

[0044] The rectangular or ovalized shape of the cup-shaped region 22 reduces the spread in the dimensions of the contact area 58 also when its shape, instead of being rectangular as in the ideal case, is oval, as may be seen from a comparison between Figure 26a, which shows the position of the cup-shaped region 22 with respect to thin region 38a in the absence of mask misalignment, and Figure 26b, which shows the relative position in presence of misalignment.

[0045] Finally, it is clear that numerous modifications and variations may be made to the process and to the memory cell described and illustrated herein, all falling within the scope of the invention, as defined in the attached claims. For example, the sequence of steps required for forming the spacer region 55a and of the strip 57 may vary. In particular, for forming the opening 51 it is possible to etch the adhesion layer 50 and the mold layer 49 alone, without removing the stop layer 48. Next, the spacer region 55a is formed in the way described previously, by depositing a spacer layer and etching it anisotropically. Finally, the stop layer 48 is removed only where it is not covered by the spacer region 55a, and in this way the strip 57 is uncovered.

[0046] In addition, according to a different embodiment, after forming the opening 51 (Figure 18) and before depositing the spacer layer 55, a protective layer 54, of silicon nitride, may be deposited, as shown in Figure 27. The protective layer 54, preferably deposited by PECVD, has, for instance, a thickness of between 20 and 30 nm. Next, etching back is performed to remove the horizontal portions of the spacer layer 55 and then the horizontal portions of the protective layer 54. A protective portion 54a thus is left only beneath the spacer region 55a, as shown in Figure 28. The protective layer 54 protects the adhesion layer 50 and prevents contamination thereof by the spacer layer 55, which is of oxide, both at the top and at the sides. In addition, it functions

as an etch stop and prevents undesired etching of the dielectric layer 20 and of the dielectric material 23 during etching back for forming the spacer region 55a.

[0047] According to a further embodiment, after depositing the adhesion layer 50 and before etching using the minitrench mask E, a further nitride layer having a thickness of 20-30 nm is deposited. Then, using the minitrench mask E, the further nitride layer, the adhesion layer 50, and the mold layer 49 are selectively removed, without the stop layer 48 being removed. The spacer layer 55 is deposited, and an etch back is performed for forming the spacer region 55a. Next, a nitride etch is carried out, removing the horizontal portions of the further nitride layer above the adhesion layer 55, and the exposed portion of the stop layer 48. Then the other steps of depositing the chalcogenic layer 38, and so forth, follow. In this way, the further nitride layer protects the adhesion layer 50 from any possible contamination by the spacer layer 55.

Claims

1. A phase change memory cell (5), comprising:

    a resistive element (22) including a first thin portion having a first sublithographic dimension in a first direction (Y); and
    a memory region (38) of a phase change material and including a second thin portion (38a) having a second sublithographic dimension in a second direction (X) transverse to said first direction;
    said resistive element (22) and said memory region (38) being in direct electrical contact at said first and second thin portions (22, 38a) and defining a contact area (58) of sublithographic extension,

    wherein said second thin portion (38a) is delimited laterally, at least in said second direction, by spacer portions (55a) of a first dielectric material, defining inclined surfaces in a third direction, transverse to said first and second directions.

2. The memory cell according to claim 1, wherein said spacer portions (55a) are surrounded by a mold layer (49) of a second dielectric material, forming a lithographic opening.

3. The memory cell according to claim 2, wherein said resistive element (22) is formed inside an insulating layer (20) of a third dielectric material, said mold layer (49) extends on top of said insulation layer, and a stop layer (48) of a fourth dielectric material extends between said insulating layer and said mold layer.

4. The memory cell according to claim 3, wherein said spacer portions (22) are of silicon dioxide, said mold layer (49) and said insulating layer are of a silicon glass, and said stop layer (48) is of silicon nitride.

5. The memory cell according to any one of claims 1 to 4, wherein said thin portion (38a) has a substantially elongated shape with a main dimension extending parallel to said first direction (Y).

6. The memory cell according to claim 5, wherein said resistive element (22) has a cup-like shape and has a vertical walls extending, in top plan view, according to a closed line chosen between a rectangular line and an elongated oval line.

7. A memory array comprising at least two memory cells (5), each of which has a respective resistive element (22) including a first thin portion having a first sublithographic dimension in a first direction (Y), said memory cells further comprising a common memory region (38) of a phase change material, said common memory region (38) comprising a second thin portion (38a) having a second sublithographic dimension in a second direction (X) transverse to said first direction; wherein said memory cells (5) are adjacent to one another in said first direction;
    the first thin region (22) of each resistive element is in direct electrical contact with said second thin region (38a) and defines a respective single contact area (58) of sublithographic extension; and
    said second thin portion (38a) is delimited laterally, at least in said second direction, by spacer portions (55a) of a first dielectric material, which define inclined surfaces in a third direction transverse to said first and second directions.

8. The memory array according to claim 7, wherein said second thin portion (38a) has an elongated shape and substantially extends along said first direction (Y).

9. A process for manufacturing a phase change memory cell, comprising:

    forming a resistive element (22) including a first thin portion having a first sublithographic dimension in a first direction (Y); and
    forming a memory region (38) of a phase change material and including a second thin portion (38a) having a second sublithographic dimension in a second direction (X) transverse to said first direction;
    said first and second thin portion (22, 38a) defining a contact area (58) of sublithographic extension;

wherein said step of forming a memory region (38) comprises forming a mold layer (49) on top of said resistive element (22); forming a first lithographic opening (51) in said mold layer; forming spacer portions (55a) in said first lithographic opening, said spacer portions defining a slit (56) having said second sublithographic dimension; and depositing a phase change layer (38) at least inside said slit.

10. The process according to claim 9, wherein said spacer portions (55a) are of a first dielectric material and have surfaces inclined in a third direction transverse to said first and second directions, and said mold layer (49) is of a second dielectric material.

11. The process according to claim 9 or 10, wherein said step of forming a resistive element (22) comprises forming a second lithographic opening (21) in an insulating layer (20), depositing a conductive layer (22) on a side wall of said second lithographic opening, and filling (23) said second lithographic opening.

12. The process according to claim 10, wherein, before said step of forming a mold layer (49), a stop layer (48) of a third dielectric material is formed on top of said resistive element (22).

13. The process according to claim 12, wherein said spacer portions (55a) are of silicon dioxide, said mold layer (49) and said insulating layer (20) are of a silicon glass, and said stop layer (48) is of silicon nitride.

14. The process according to any one of claims 9 to 13, wherein said second thin portion (38a) has a substantially elongated shape and extends parallel to said first direction (Y) .

15. The process according to any one of claims 9 to 14, wherein said resistive element (22) has a cup-like shape and has a vertical side that extends, in top plan view, according to a closed line chosen between a rectangular line and an elongated oval line.

16. The process according to any one of claims 9 to 15, wherein said step of forming spacer portions (55a) comprises, after said step of forming a first lithographic opening (51), the steps of depositing a spacer layer (55) and anisotropically etching said spacer layer.

17. The process according to any one of claims 9 to 16, wherein, before said step of forming a first lithographic opening (51), the step of depositing an adhesion layer (50) is carried out.

18. The process according to claim 17, wherein said step of forming spacer portions (55a) comprises depositing a protective layer (54), depositing a spacer layer (55), anisotropically etching said spacer layer, and selectively removing said protection layer above said adhesion layer (50) and at the sides of said spacer portions in said first lithographic opening.

19. A process for forming a pair of memory cells (5) adjacent in a first direction (Y), comprising the steps of:

forming a pair of resistive elements (22) each of which includes a first thin portion having a first sublithographic dimension in a first direction (Y); and
forming a common memory region (38) of a phase change material and including a second thin portion (38a) in direct electrical contact with said first thin portions and having a second sublithographic dimension in a second direction (X) transverse to said first direction;
each resistive element forming, with said second thin portion, a respective contact area (58) of sublithographic extension;

wherein said step of forming a common memory region (38) comprises forming a mold layer (49) on top of said resistive elements (22); forming a first lithographic opening (51) in said mold layer, said lithographic opening extending between said pairs of resistive elements (22) above said first thin portion of said pair of resistive elements; forming spacer portions (55a) in said lithographic opening, said spacer portions defining a slit (56) having said second sublithographic dimension; and depositing a phase change layer (38) at least inside said slit.

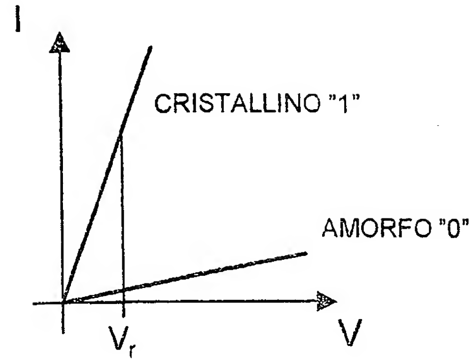


Fig.1

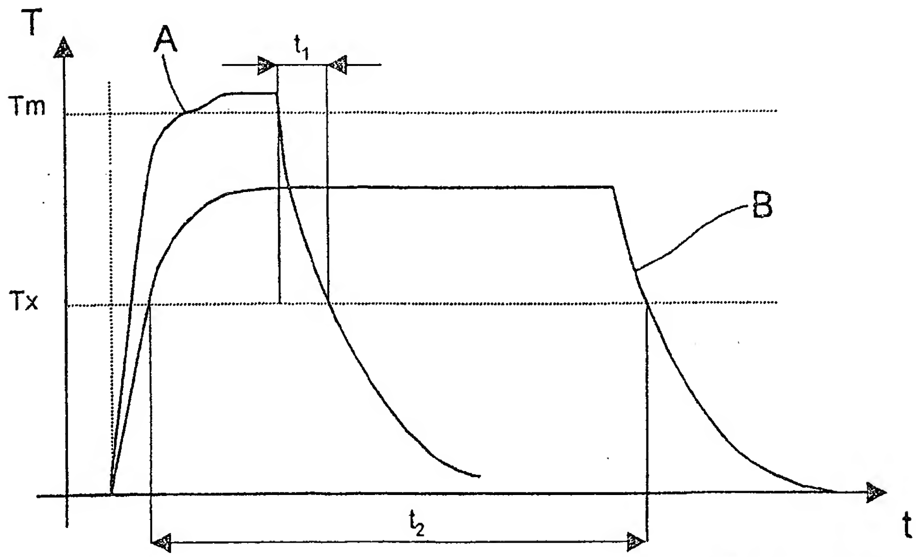


Fig.2

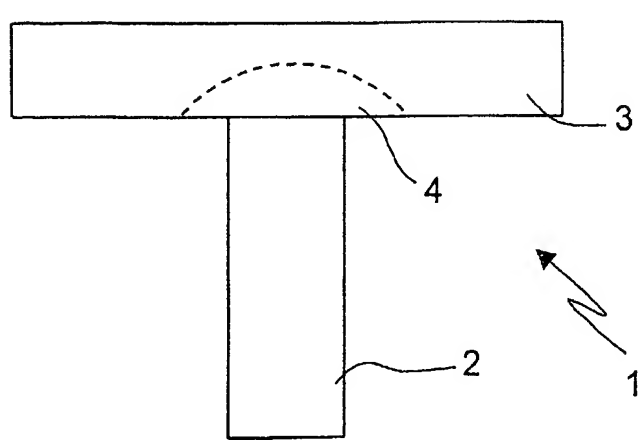


Fig.3

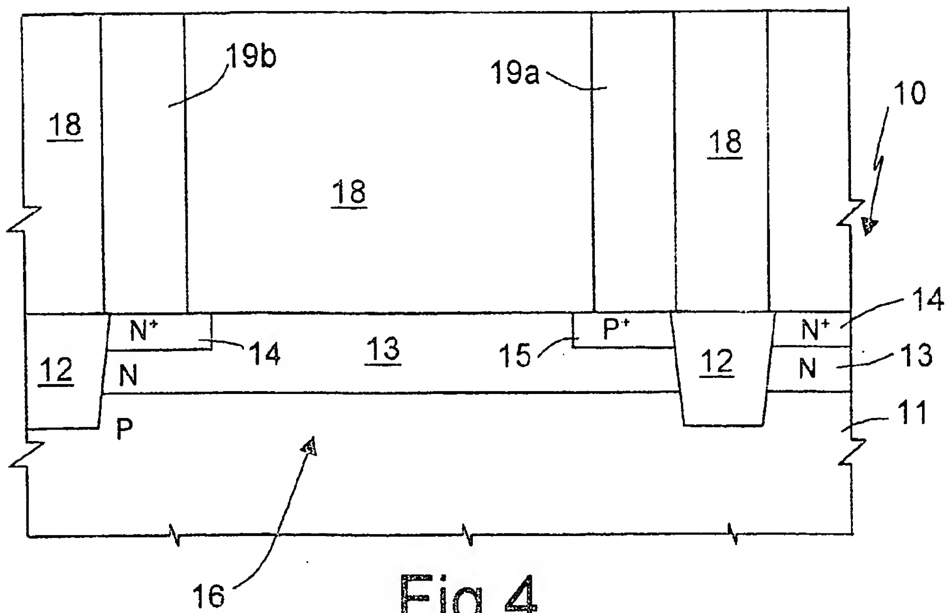


Fig.4

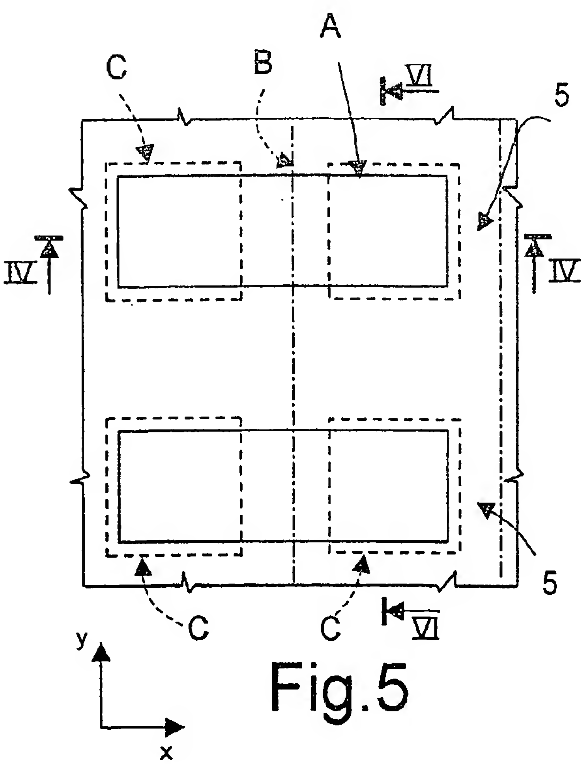
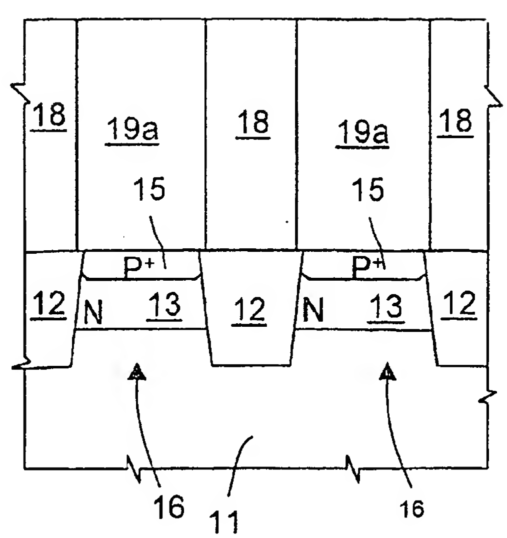


Fig.5



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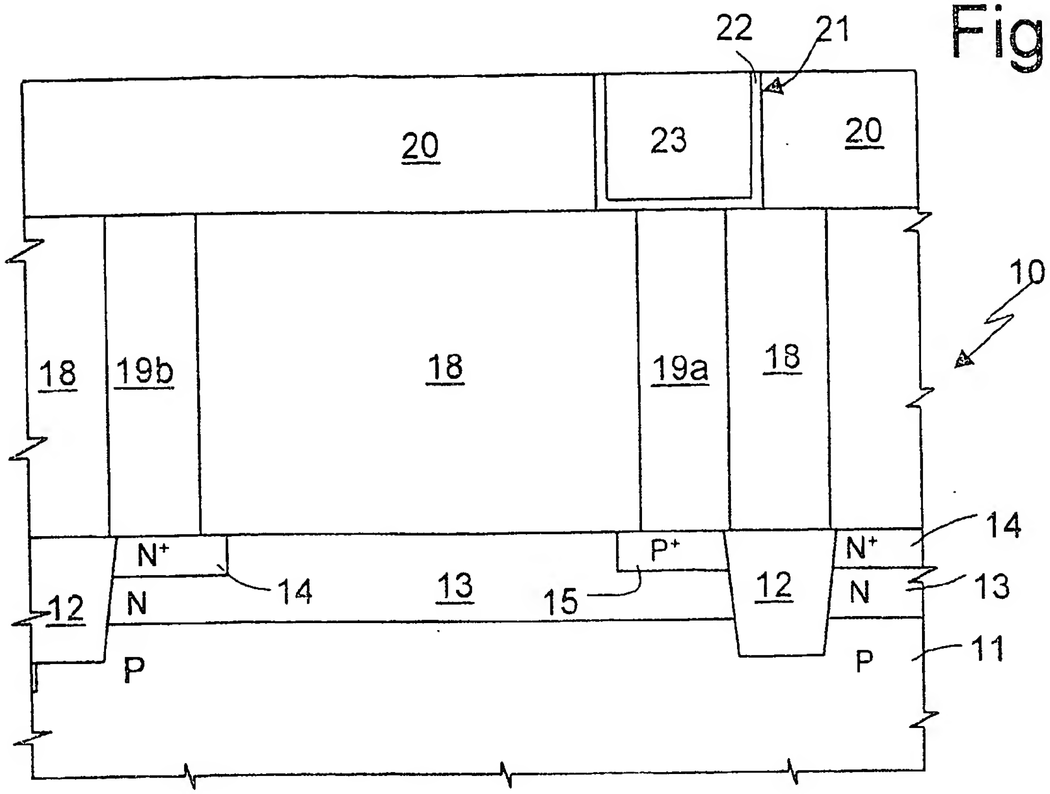
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Fig.7

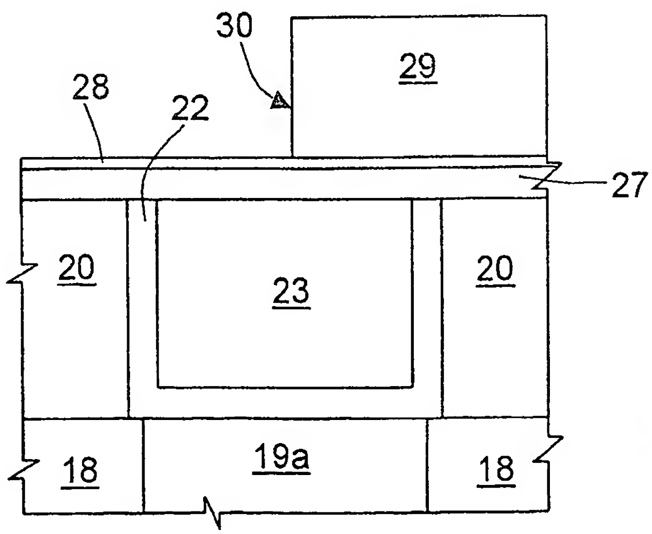
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Fig.8

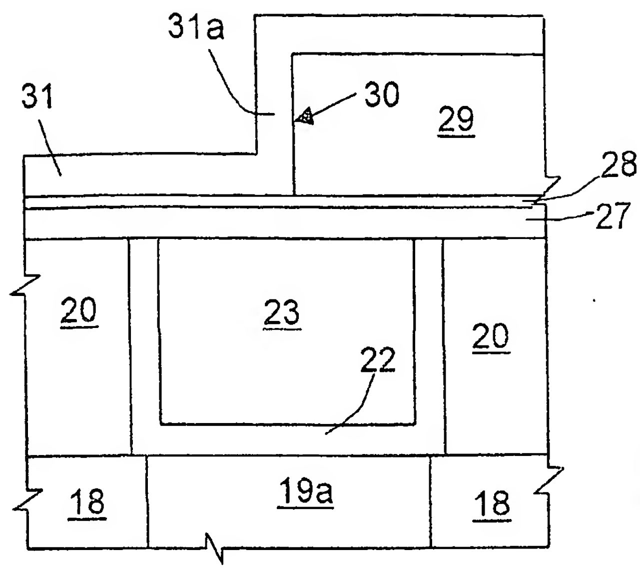

Fig.9

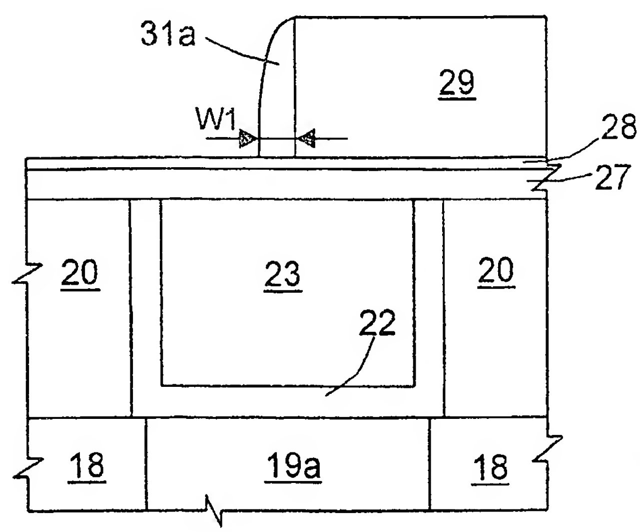

Fig.10

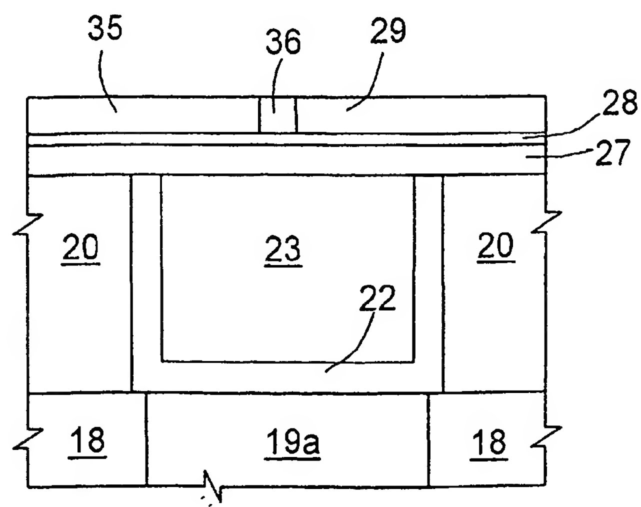

Fig.11

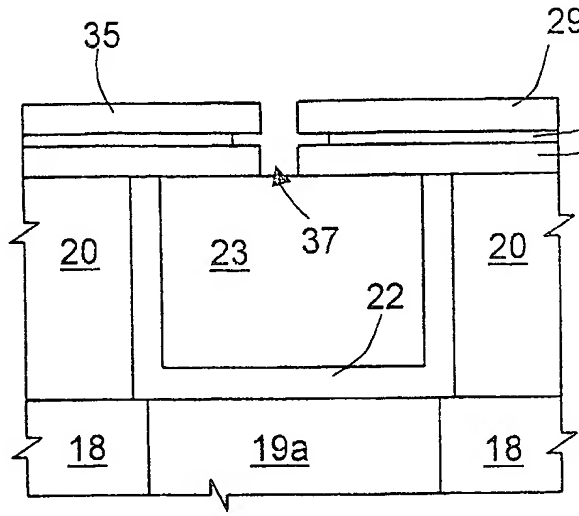
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Fig.12

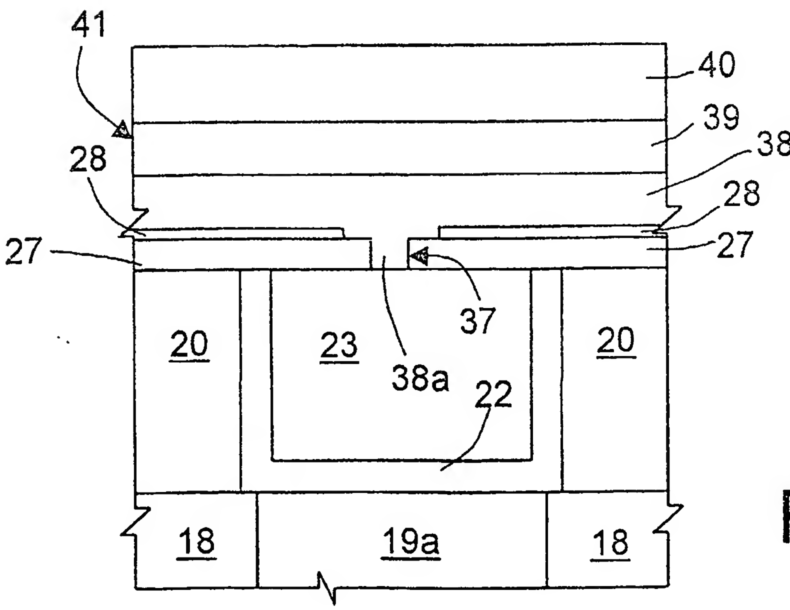
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Fig.13

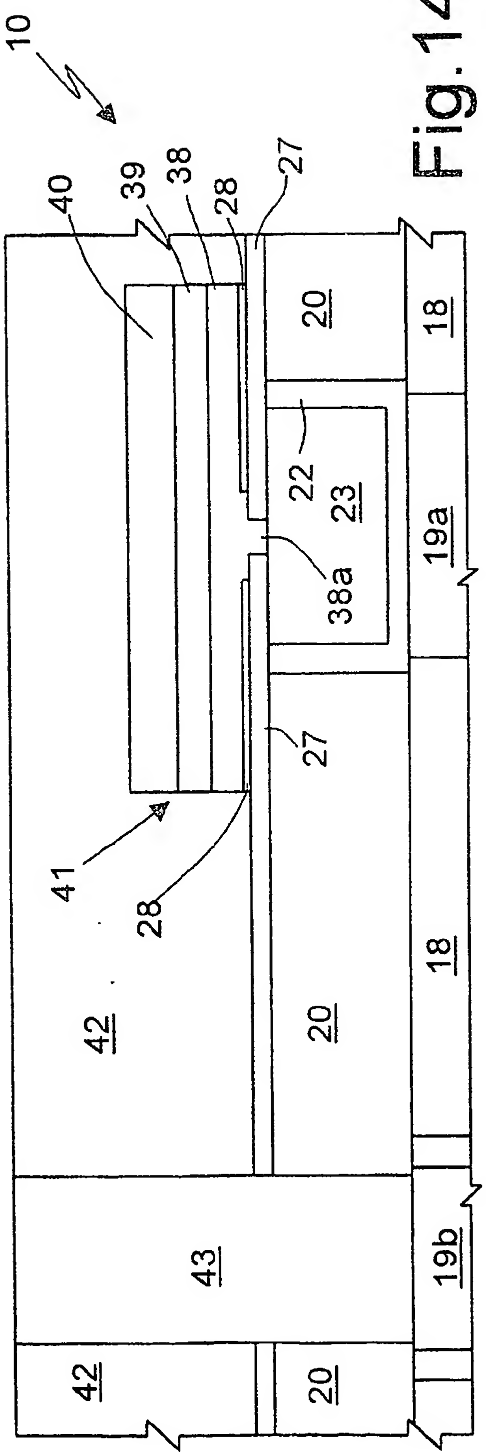

Fig. 14

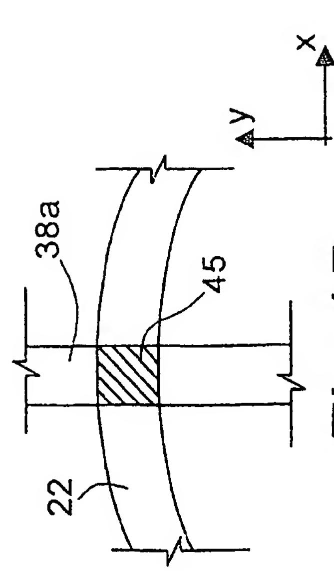

Fig. 15

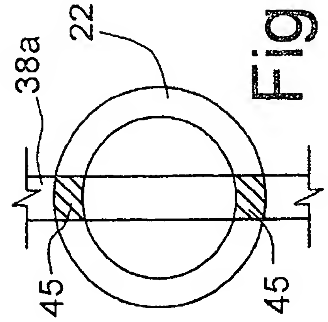

Fig. 16a

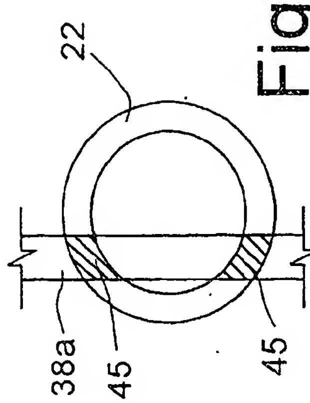

Fig. 16b

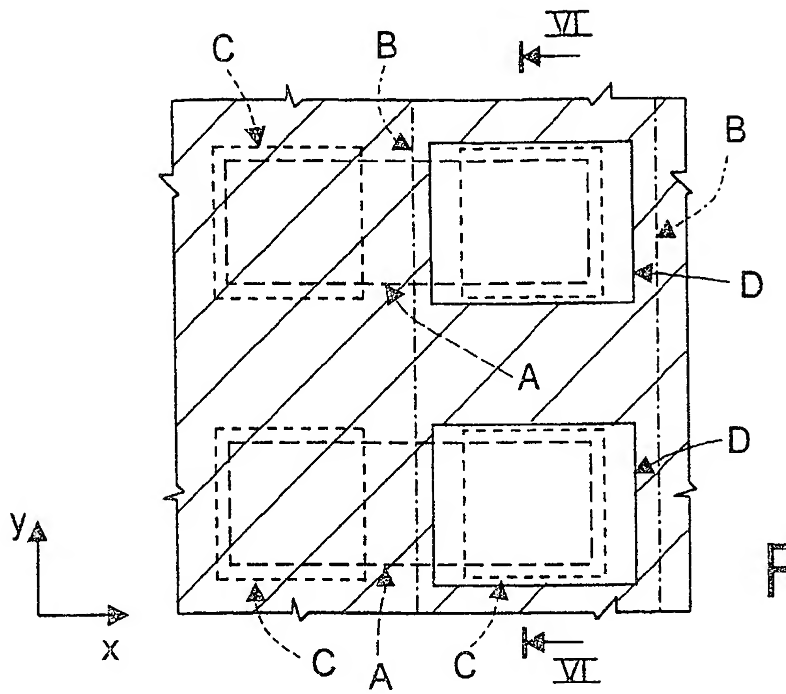

Fig.17

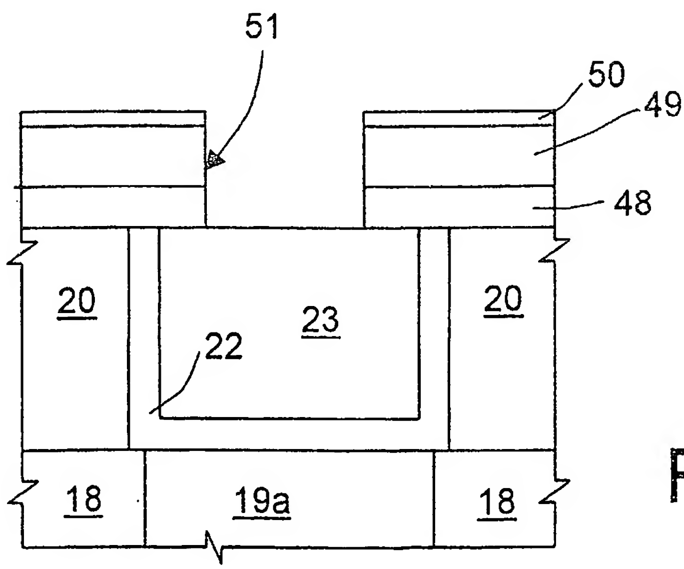

Fig.18

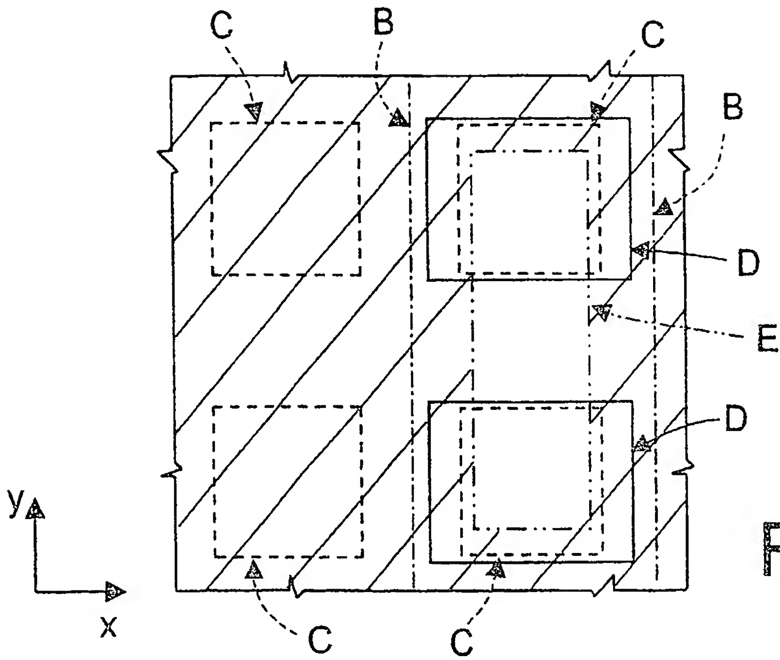

Fig.19

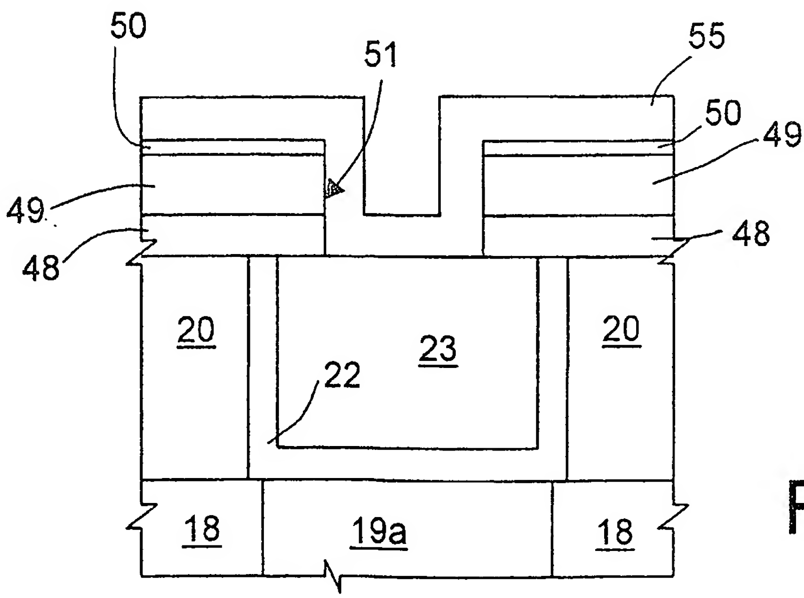

Fig.20

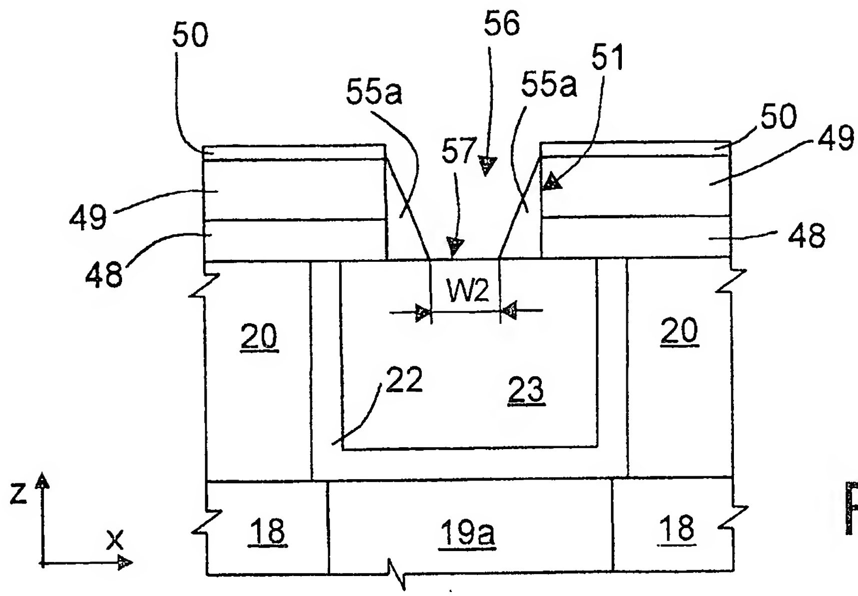
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Fig.21

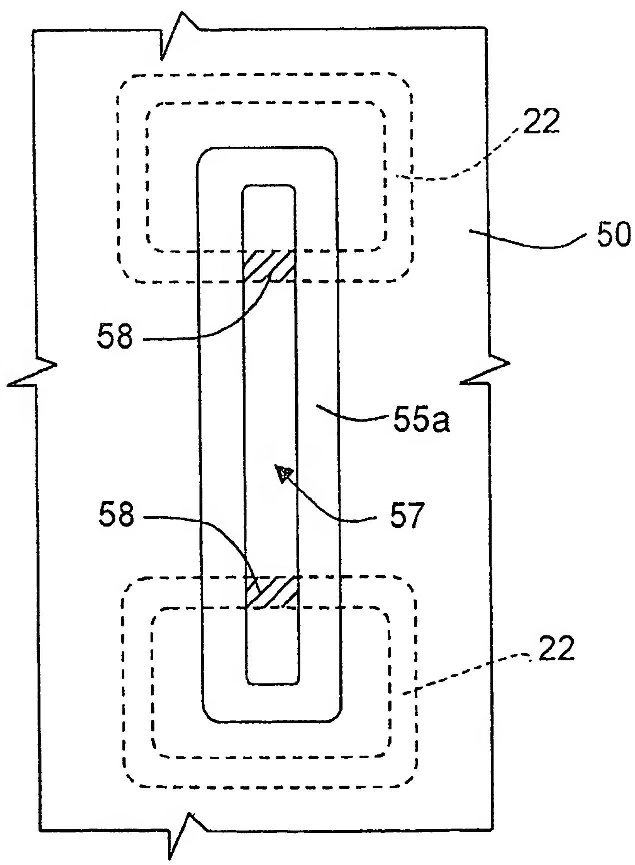
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Fig.22

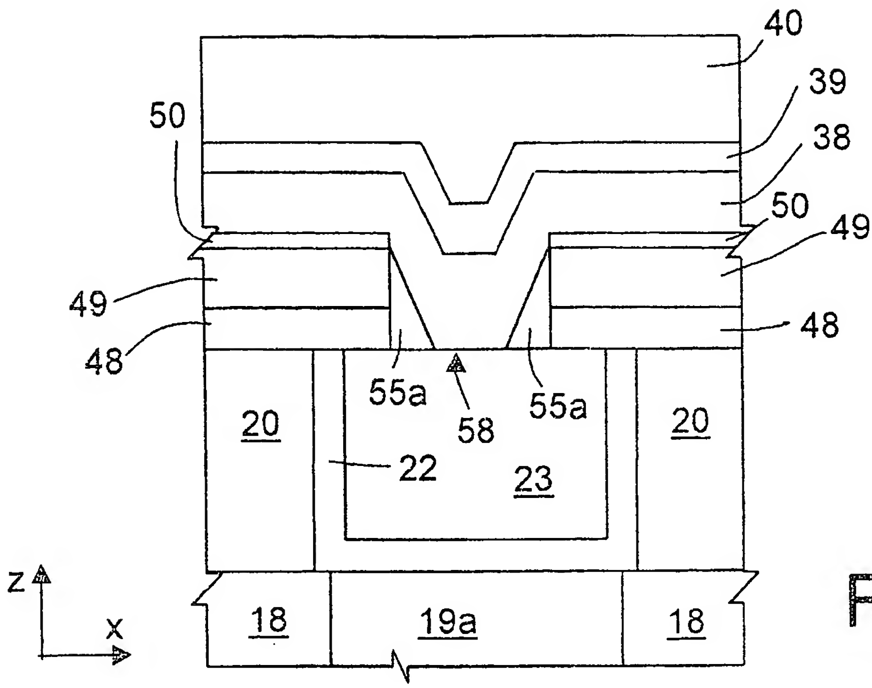
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Fig.23

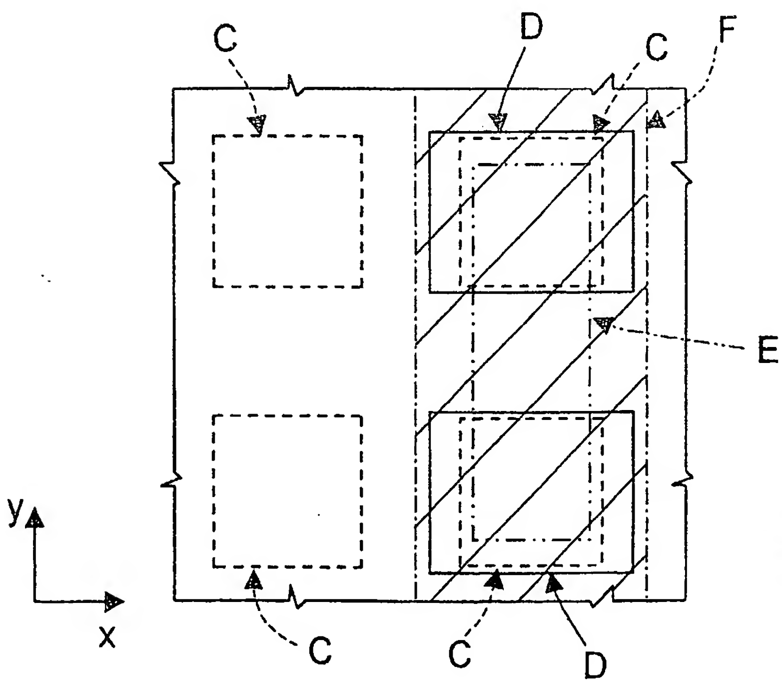
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Fig.24

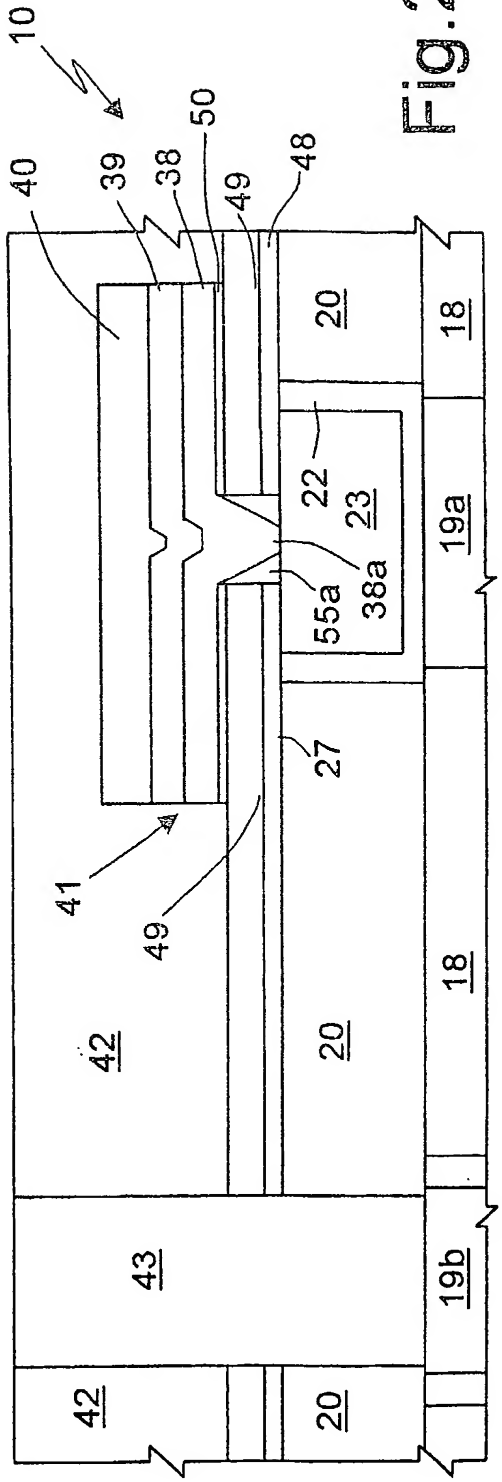
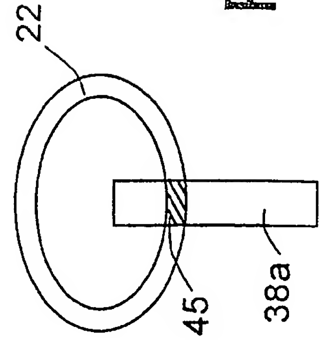


Fig.25



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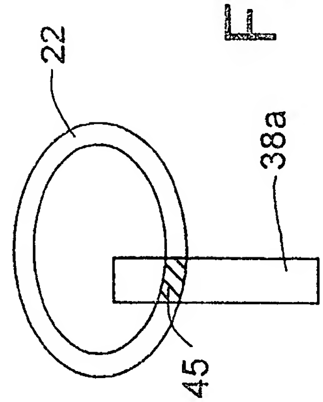

Fig.26b

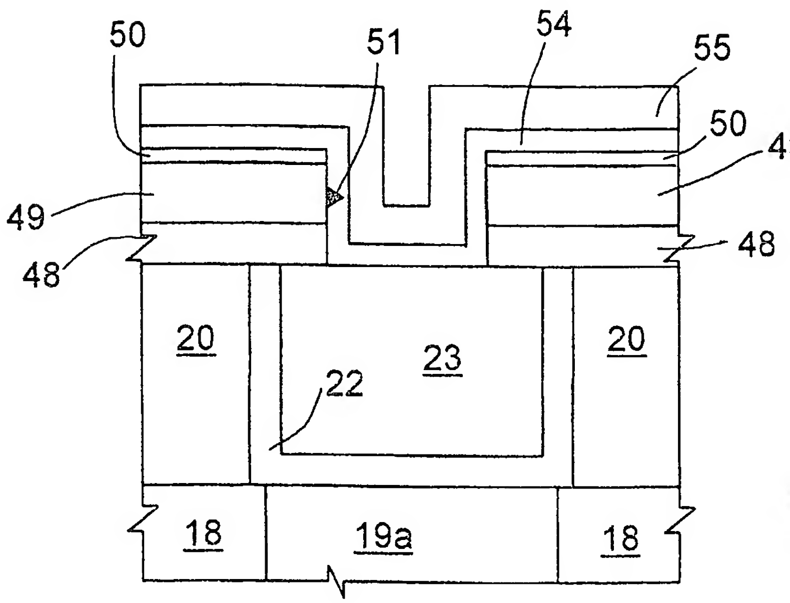
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Fig.27

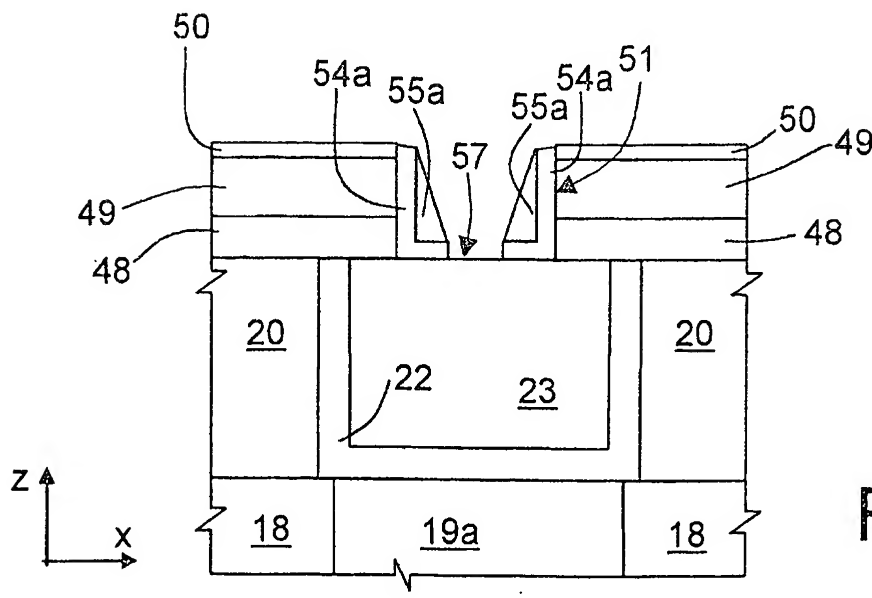
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Fig.28

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 42 5087

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Y	US 6 031 287 A (HARSHFIELD STEVEN T) 29 February 2000 (2000-02-29)	1,2,5, 9-11,14, 16	H01L45/00 H01L27/24
A	* column 15, line 7 - column 16, line 13; figures 26-31 *	3,6-8, 15,19	
Y	US 2002/017701 A1 (KLERSY PATRICK ET AL) 14 February 2002 (2002-02-14)	1,2,5, 9-11,14, 16	
A	* paragraph '0037! - paragraph '0062!; figures 4-13 *	3,6,15	
A	WO 02 09206 A (OVONYX INC) 31 January 2002 (2002-01-31) * page 11, line 9 - page 46, line 27 * * page 51, line 11 - page 79, line 12 * * figures 1-6,9-14 *	1,5-9, 11,14, 15,19	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
			H01L G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	12 August 2002	Köpf, C

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12-08-2002

Patent document cited in search report		Publication date	Patent family member(s)			Publication date
US 6031287	A	29-02-2000	NONE			
US 2002017701	A1	14-02-2002	AU	3769900	A	09-10-2000
			BR	0009308	A	18-12-2001
			CN	1352808	T	05-06-2002
			EP	1171920	A1	16-01-2002
			WO	0057498	A1	28-09-2000
			US	2002036931	A1	28-03-2002
			US	2002045323	A1	18-04-2002
WO 0209206	A	31-01-2002	US	2002045323	A1	18-04-2002
			AU	7597101	A	05-02-2002
			WO	0209206	A1	31-01-2002
			US	2002036931	A1	28-03-2002

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